REJECTION OF CLAIM 1 UNDER 35 U.S.C. §102

Claim 1 has been rejected under 35 U.S.C. 102 as being anticipated by Mizura, IDS reference CM (IBM Technical Disclosure Bulletin), Mikami, and Chikyow. The two remaining independent claims 1 and 9 have been amended to overcome the references as discussed during the interview.

Accordingly, it is believed that the rejection of claims 1 and 9 under 35 U.S.C. 102 has been overcome by the amendment and remarks.

REJECTION OF CLAIMS 2-6, 8-10, 12, AND 13 UNDER 35 U.S.C. §102

Claims 2-6, 8-10, 12, and 13 have been rejected under 35 U.S.C. 102 as being anticipated by Mizura

The dependant claims are believed allowable since they add further limitations to the independent claims 1 and 9.

Accordingly, it is believed that the rejection of claims 2-6, 8-10, 12, and 13 under 35 U.S.C. 102 has been overcome by the amendment and remarks.

ALLOWABLE CLAIMS

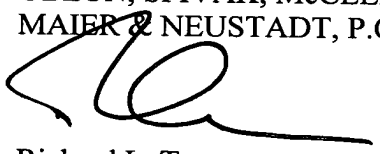
Claims 7 and 11 have been identified as being allowable, but objected to as being dependent upon a rejected base claim. The rejected base claims have been amended and are believed allowable.

Accordingly, it is believed that the objection to claims 7 and 11 has been overcome by the amendment and remarks.

In view of the above, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections is requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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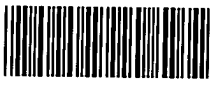

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MARKED-UP COPY OF SPECIFICATION AND CLAIMS
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE SPECIFICATION

On page 1, line 1, change the title to "FET WITH AMORPHOUS GATE INSULATION LAYER--.

On page 12, line 1, change the title to "FET WITH AMORPHOUS GATE INSULATION LAYER--.

IN THE CLAIMS

1. A semiconductor device, comprising:

a semiconductor substrate; and

a dielectric layer formed over the semiconductor substrate and having a first portion formed with an amorphous material and a second portion formed with a monocrystalline pervoskite material, where an electric field in the dielectric layer controls a conductivity of the semiconductor substrate.

9. A transistor, comprising:

a substrate;

a gate electrode disposed over the substrate for generating a conduction channel in the substrate in response to a control signal; and

a dielectric formed over the conduction channel, the dielectric including a first layer formed with an amorphous material, a second layer formed with a monocrystalline pervoskite material disposed between the first layer and the gate electrode.